

ABSTRACT OF THE DISCLOSURE**SYMMETRIC MULTIPROCESSING (SMP) SYSTEM WITH
FULLY-INTERCONNECTED HETEROGENOUS MICROPROCESSORS**

Disclosed is a fully-interconnected, heterogenous, multiprocessor data processing system. The data processing system topology has a plurality of processors each having unique characteristics including, for example, different processing speeds (frequency) and different cache topologies (sizes, levels, etc.). Second and third generation heterogenous processors are connected to a specialized set of pins, connected to the system bus. The processors are interconnected and communicate via an enhanced communication protocol and specialized SMP bus topology that supports the heterogeneous topology and enables newer processors to support full downward compatibility to the previous generation processors. Various processor functions are modified to support operations on either of the processors depending on which processor is assigned which operations. The enhanced communication protocol, operating system, and other processor logic enable the heterogenous multiprocessor data processing system to operate as a symmetric multiprocessor system.